EAST - [10795890B.wsp:1]

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  - L1: (5) "6657229"
  - L2: (1) ("6657229").PN.
  - L3: (1) ("5182225").PN.
  - L4: (4182) (MOS or BICMOS) and anneal and polysilicon
  - L6: (7) (BICMOS) and anneal and polysilicon and hydrogen near ambient
  - L5: (860) (BICMOS) and anneal and polysilicon
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Default operator: OR | Highlight all hit terms initially

(BICMOS) and anneal and polysilicon

BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
798	☐	☐	US 5198387 A	19930330	16	Method and apparatus for in-situ doping of deposited silicon	438/684	257/E21.101; 257/E21.297; 257/E21.396;
799	☐	☐	US 5192708 A	19930309	7	Sub-layer contact technique using in situ doped amorphous silicon and solid phase recrystallization	438/361	148/DIG.50; 257/E21.133; 257/E21.538;
800	☐	☐	US 5182225 A	19930126	66	Process for fabricating BICMOS with hypershallow junctions	438/202	257/276; 257/370; 257/371;
801	☐	☐	US 5181095 A	19930119	25	Complementary bipolar and MOS transistor having power and logic structures on the same integrated circuit substrate	257/370	257/556; 257/E27.015
802	☐	☐	US 5171713 A	19921215	67	Process for forming planarized, air-bridge interconnects on a semiconductor substrate	438/31	148/DIG.20; 257/750; 257/E21.166;
803	☐	☐	US 5171702 A	19921215	13	Method for forming a thick base oxide in a BiCMOS process	438/207	148/DIG.9; 257/E21.166; 257/E21.375;
804	☐	☐	US 5171699 A	19921215	19	Vertical DMOS transistor structure built in an N-well CMOS-based BiCMOS process and method of fabrication	438/206	257/E21.418; 257/E21.544; 257/E21.632;
805	☐	☐	US 5169794 A	19921208	11	Method of fabrication of pnp structure in a common substrate containing npn or MOS structures	438/203	257/370; 257/565; 257/E21.696;
806	☐	☐	US 5166770 A	19921124	14	Silicided structures having openings therein	257/770	257/773; 257/E21.16; 257/E23.163;
807	☐	☐	US 5158900 A	19921027	9	Method of separately fabricating a base/emitter structure of a BiCMOS device	438/202	257/E21.696; 438/207
808	☐	☐	US 5155571 A	19921013	8	Complementary field effect transistors having strained superlattice structure	257/19	257/370; 257/E27.012; 257/E27.062;

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